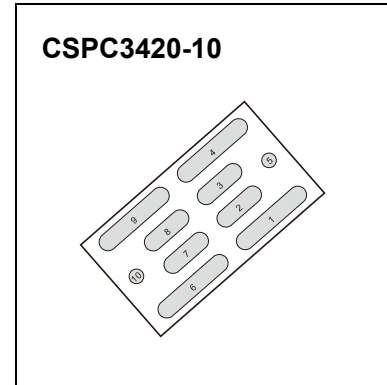




CSP Enhancement Mode Power MOSFET

8618SP Dual N-Channel MOSFET

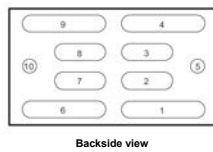
V _{SSS}	R _{SS(on)} TYP	I _S
23V	3.2mΩ@4.5V	13A
	3.3mΩ@3.8V	
	3.5mΩ@3.1V	
	3.8mΩ@2.5V	



DESCRIPTION

The 8618SP uses advanced trench technology to provide excellent R_{SS(ON)}, low gate charge and operation with gate voltages as low as 2.5V while retaining a 8V V_{GS(MAX)} rating. It is ESD protected. This device is suitable for use as a unidirectional or bi-directional load switch, facilitated by its common-drain configuration.

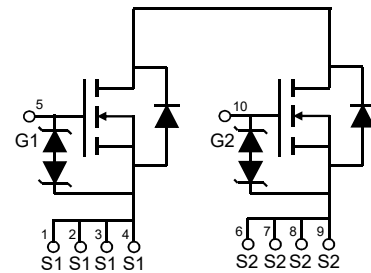
Marking and pin assignment



Marking:

- | | |
|-----------------------|--------------------|
| 1. 8618: Product Code | 1, 2, 3, 4 Source1 |
| 2. YYMMX: Date Code | 6, 7, 8, 9 Source2 |
| 3. Solid dot: Pin 1 | 5 Gate1 |
| | 10 Gate2 |

Equivalent Circuit



ABSOLUTE MAXIMUM RATINGS (T_a=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Source to Source Voltage	V _{SSS}	23	V
Gate-Source Voltage	V _{GSS}	±8	V
Source Current(DC)	I _S ^①	13	A
Source Current (Pulsed)	I _{SP} ^①	130	A
Total Power Dissipation	P _T ^①	3.1	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature Range	T _{STG}	-55 To 150	°C

MOSFET ELECTRICAL CHARACTERISTICS

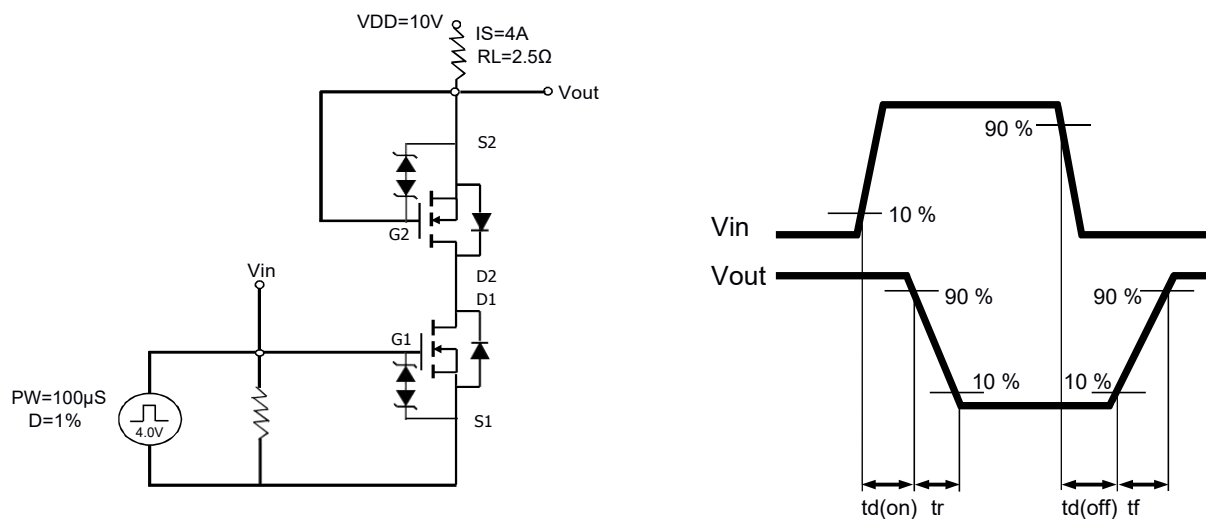
$T_a=25\text{ }^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Parameters						
Source to Source Breakdown Voltage	BV_{SSS}	$I_S=1\text{mA}, V_{GS}=0\text{V}$	23			V
Zero-Gate Voltage Source Current	I_{SSS}	$V_{SS}=19\text{V}, V_{GS}=0\text{V}$			100	nA
Gate to Source Leakage Current	I_{GSS}	$V_{SS}=0\text{V}, V_{GS}=\pm 8\text{V}$			± 10	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	$V_{SS}=V_{GS}, I_S=1.31\text{ mA}$	0.4	0.77	1.4	V
Source to Source On-state Resistance	$R_{SS(on)}$	$V_{GS}=4.5\text{V}, I_S=6.5\text{A}$	0.5	3.2	4.0	$\text{m}\Omega$
		$V_{GS}=3.8\text{V}, I_S=6.5\text{A}$	0.5	3.3	4.2	$\text{m}\Omega$
		$V_{GS}=3.1\text{V}, I_S=6.5\text{A}$	0.5	3.5	4.8	$\text{m}\Omega$
		$V_{GS}=2.5\text{V}, I_S=6.5\text{A}$	0.5	3.8	7.2	$\text{m}\Omega$
Input Capacitance	C_{iss}	$V_{SS}=10\text{V}, V_{GS}=0\text{V}, f=100\text{kHz}$		1010		pF
Output Capacitance	C_{oss}			445		pF
Reverse Transfer Capacitance	C_{rss}			68		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=10\text{V}, R_L=2.5\Omega, V_{GS}=4.0\text{V}$		0.73		μs
Turn-on Rise Time	t_r			1.73		μs
Turn-off Delay Time	$t_{d(off)}$			9.08		μs
Turn-off Fall Time	t_f			3.36		μs
Total Gate Charge	Q_g	$V_{SS}=10\text{V}, I_S=4\text{A}, V_{GS}=8\text{V}$		69		nC
Gate1-source1 charge	Q_{g1s1}			6.8		nC
Gate1-source2 charge	Q_{g1s2}			10		nC
Diode Forward Voltage	$V_{F(S-S)}$	$V_{GS}=0\text{V}, I_S=6\text{A}$			1.0	V

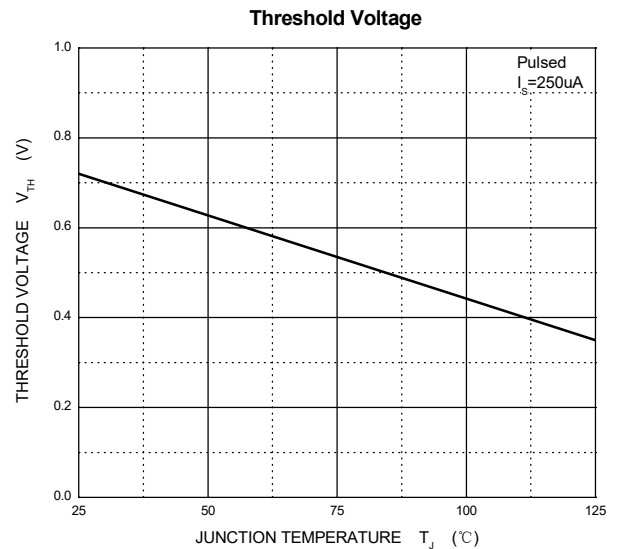
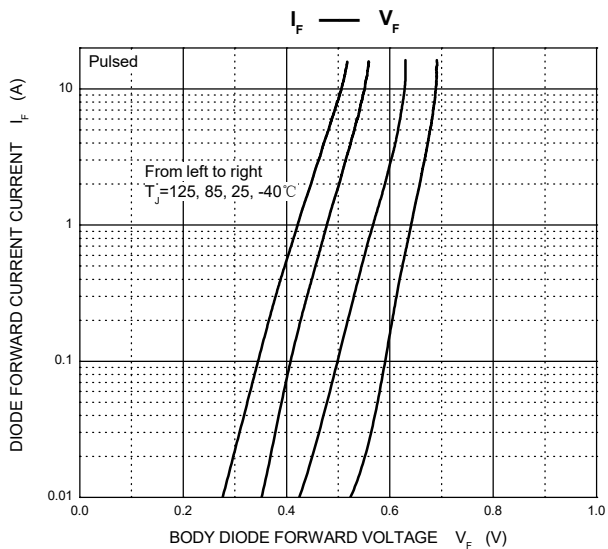
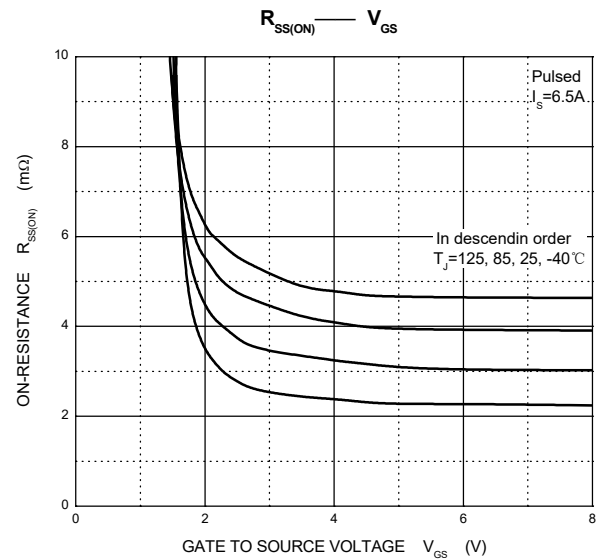
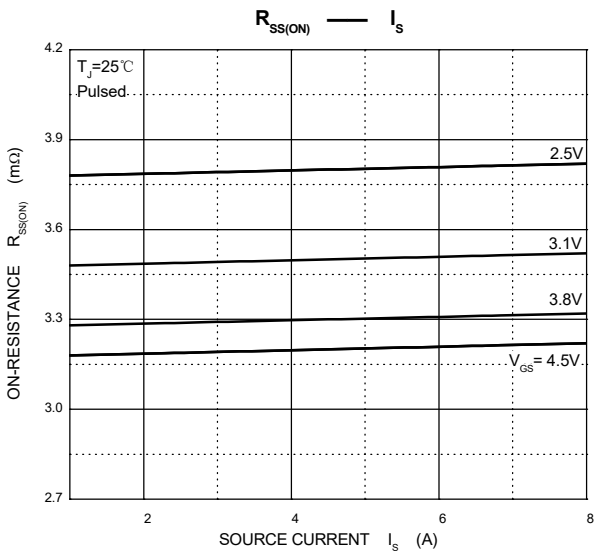
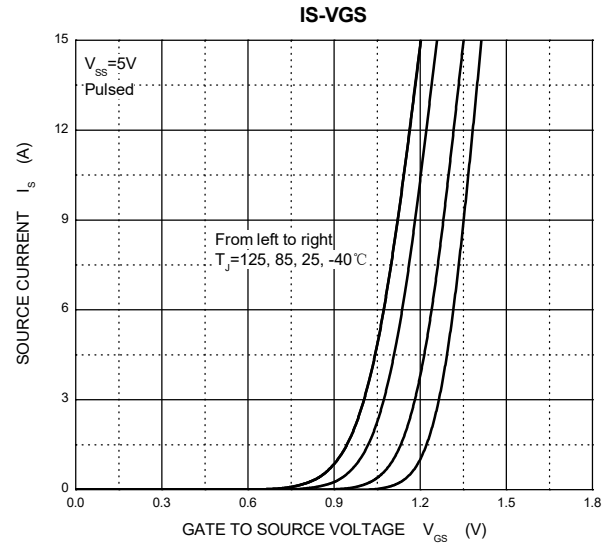
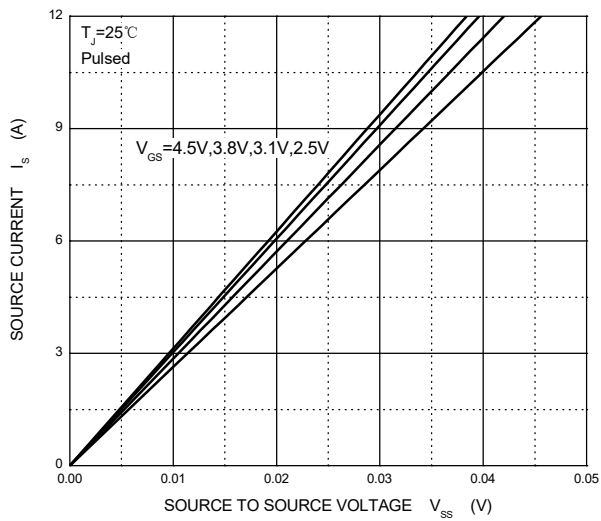
Notes: 1. Mounted on FR4 board (25.4mm×25.4mm×1.0mm) using the minimum recommended pad size (36um Copper).

2. $t = 10\text{ ms}$, Duty Cycle = 1 %.

3. When FET1 is measured, G2 and S2 are short-circuited.

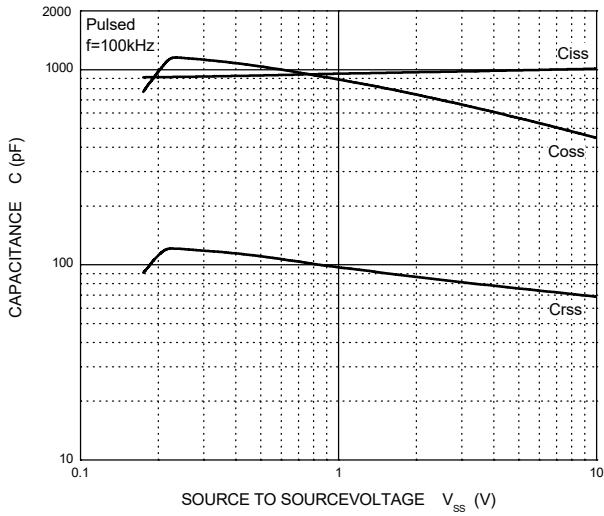


Typical Characteristics

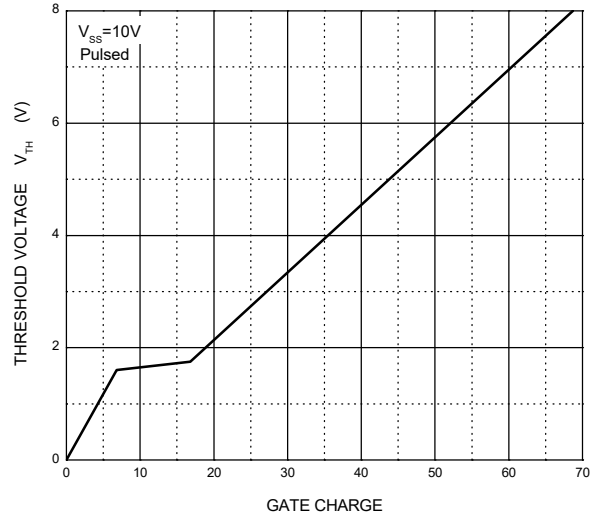


Typical Characteristics

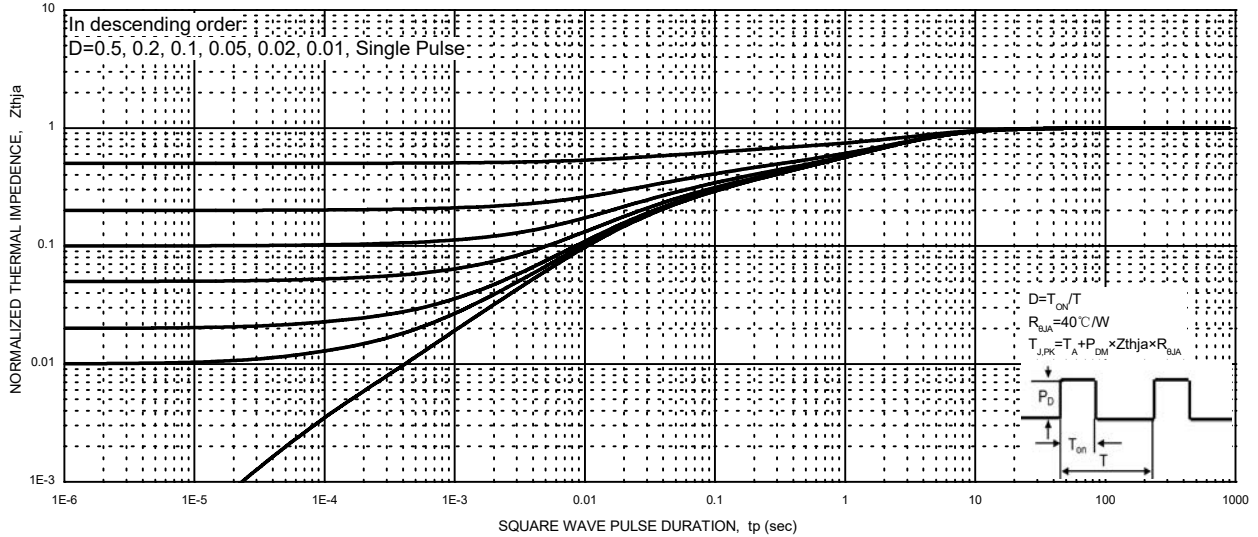
Capacitances



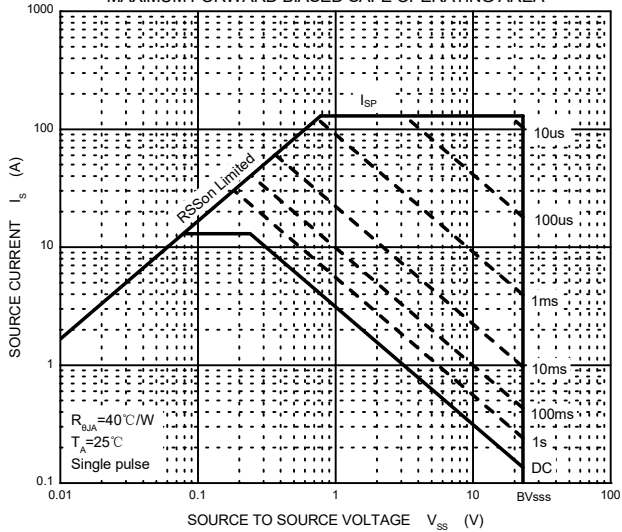
Gate Charge



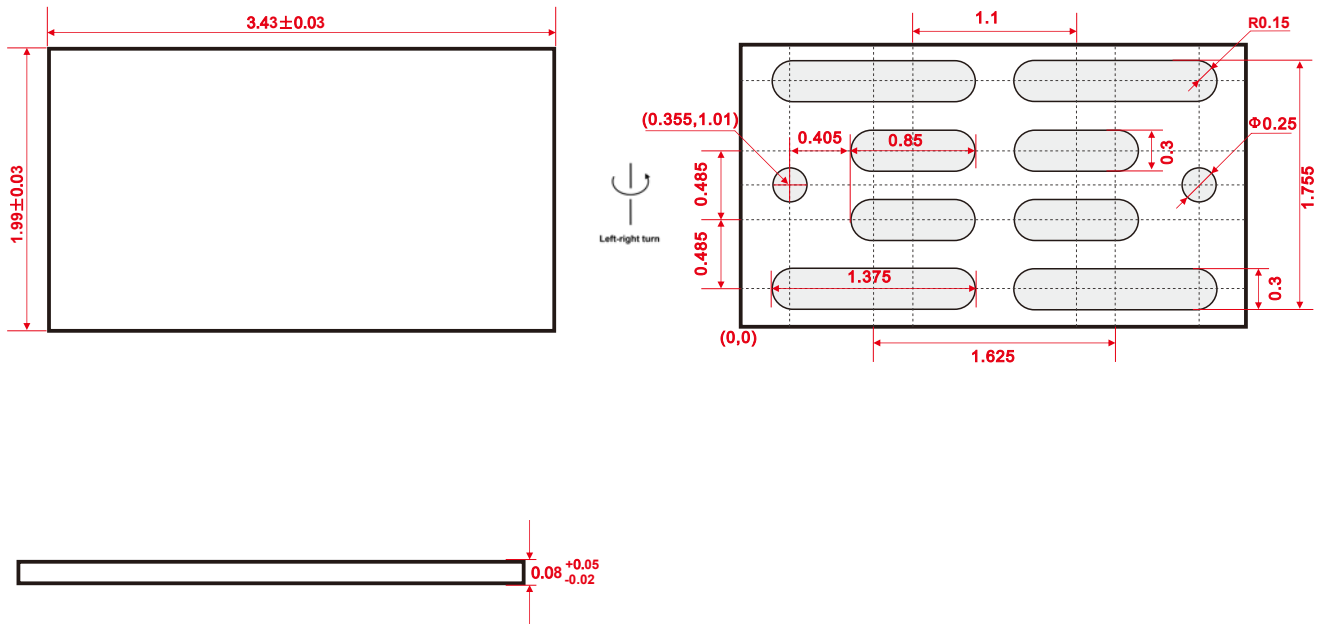
NORMALIZED TRANSIENT THERMAL IMPEDANCE



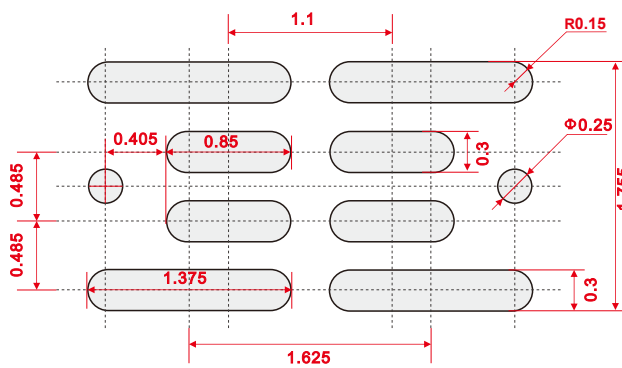
MAXIMUM FORWARD BIASED SAFE OPERATING AREA



CSPC3420-10 Package Outline Dimensions(Unit:mm)



CSPC3420-10 Suggested Pad Layout (Unit:mm)



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.050 mm.
3. The pad layout is for reference purposes only.

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